A RF-MEMS Based Tunable Matching Network for 2.45-GHz Discrete-Resizing CMOS Power Amplifiers

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Abstract. *This paper deals with the design and experimental validation of a tunable matching network for discrete-resizing CMOS power amplifiers operating at 2.45 GHz (i.e. in the WiFi frequency band). The network is based on a two stages ladder configuration and exploits high-Q MEMS capacitors to achieve the impedance tuning. Furthermore, since these capacitors can be programmed through a 3-wires serial interface, a fully digital control of the transformed impedance is achieved.*

Keywords

Power Amplifiers (PA), Envelope Tracking (ET), discrete-resizing, CMOS, Tunable Matching Networks (TMN), MEMS capacitors, reconfigurable front-ends, WLAN.

1. Introduction

Power Amplifiers (PAs) are one of the key building blocks for wide-band mobile terminals, affecting both the linearity and the power efficiency of the whole RF front-end. In modern wireless communication systems, indeed, non-constant envelope schemes are exploited in order to achieve a high data rate. As a consequence, the efficiency to linearity trade-off very challenging. For example, the WLAN 802.11n standard employs 64 Quadrature Amplitude Modulation (QAM) and Orthogonal Frequency-Division Multiplexing (OFDM) carriers. These modulation formats have a high envelope Peak-to-Average Ratio (PAR) of 8–10 dB, determining the condition that average efficiency is much lower than the peak efficiency [1].

To deal with the efficiency-linearity bottleneck one trend is to provide a direct digital modulation either in I/Q [2] or polar domains [3]-[5]. Linearisation and pre-distortion seem to be mandatory with nano-scale CMOS devices [6, 7]. Furthermore, adaptive matching networks have been also used to optimize the PA performance over different frequency bands. These networks are implemented either exploiting a RF-MEMS process [8] or in the same CMOS technology adopted for the PA [9].

On the other hand, in order to achieve a high miniaturization level and to limit the Bill-of-Material (BoM) to less than about 100 components, RF and microwave front-ends should exploit integrated circuits, multi-mode and multi-standard operation [10, 11] and reconfigurability [12] whenever is possible. From this point of view, the best solution is to adopt the System-on-Chip (SoC) approach in both nano-scale CMOS or SiGe BiCMOS technologies, such as those reported in [13]-[15]. However, although SoC is perfect for the digital part of the transceiver and for most of the microwave sections (i.e. the active ones), it is not optimal when low-loss and passive sub-circuits are considered. Among these circuits, the output matching network plays a very important role for PAs.

In the above scenario, one of the most effective methods for the PA efficiency enhancement is constituted by the Envelope Tracking (ET) technique [16, 17]. The ET is basically achieved by adjusting the supply voltage of the amplifier (and thus its 1 dB compression point) in order to track the long-term average of the envelope signal. With such an approach, the PA can operate with a good trade-off between efficiency and linearity [18], (at least for a certain range of input signal envelopes), thus improving the average power efficiency.

The signal envelope can be followed in a continuous way or using a multiple level waveform. Furthermore, instead of varying the PA supply voltage, also the size of the power transistors can be varied. This configuration, known as discrete-resizing PA, has the advantage of not requiring a complex supply voltage regulator and can be easily implemented as a SoC together with the other circuits of the transceiver [19]-[21]. In these amplifiers the 1 dB compression point is increased, with a constant supply voltage, by increasing the transistor size. As a consequence, accord-

ing to the load-line theory and assuming an AB-class operation, the optimum termination impedance must be decreased. This means that, as a function of the signal envelope, one has to adjust, in discrete steps, both the transistor size and the output matching network. Low-loss Tunable Matching Networks (TMNs) are thus of fundamental importance for discrete-resizing PAs.

In this work, for the first time, a ladder TMN (two L networks in cascade), based on digitally-controlled commercial RF-MEMS capacitors [22, 23], is designed and experimentally validated. The network is suitable for an ET discrete-resizing PA operating at 2.45 GHz (WLAN applications). Such a PA is designed exploiting a 65 nm CMOS technology and uses a resizing from 1 (nominal transistor width) to 7 (i.e. 7 times the nominal transistor width). This means that the TMN has the very hard task of reconfiguring the load impedance in a wide range of values (from the optimum load impedance corresponding to the nominal transistor width to about 1/7 of this value). Previous examples of TMN for PA can be found in the literature. In [8] RF-MEMS capacitors were used but the network had a very simple configuration and was only intended to compensate the mismatch between antenna and transmitter. It operates at 900 MHz for Code Division Multiple Access (CDMA) applications. In [24] a two-stage ladder network has been proposed but it is based on varactor devices. Such a network operates up to 2.1 GHz and is not intended for discrete-resizing transistors. Finally, TMN exploiting on-chip transformers are also reported in [9, 20]. The advantage of these designs is that of going in the direction of a fully integrated transmitter front-end. However these circuits suffer for high insertion losses, i.e. greater than about 1.4 dB in the best case, [9] or for a limited range of tuned impedances, [20].

The paper is organized as follows. In Sec. 2 the discrete-resizing PA concept is described and the optimum load impedances for the different transistor states are simulated. Then, in Sec. 3, the TMN design is presented. Such a design starts from the optimum PA impedances and exploits the digitally-controlled RF-MEMS capacitors from CK. The experimental results are reported in Sec. 4 and, finally, Sec. 5 is devoted to the conclusions.

2. PA Concept

The architecture of the proposed Envelope-Tracking (ET) power amplifier is shown in Fig. 1. It is based on a discrete-resizing PA core (in particular the power transistors of the final stage) and on a TMN that can be reconfigured to follow the signal envelope. In order to accommodate the amplitude modulation peaks, a typical class AB power amplifier is usually operated in back-off condition (at least with 6 dB), thus wasting a lot of DC power. On the contrary, with the architecture of Fig. 1, the 1 dB compression point of the amplifier is varied to follow the signal envelope, thus requiring a high DC power only during the peaks. As a consequence the Power Added Efficiency (PAE) can be kept high also in the average operation of the circuit.

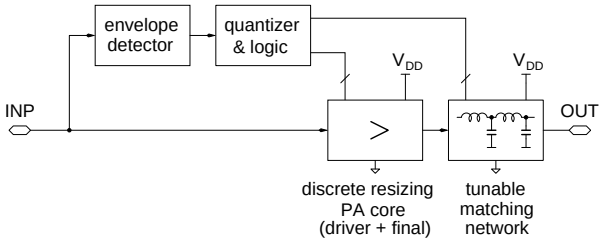


Fig. 1. Block diagram of the proposed ET power amplifier based on discrete resizing. Both the PA core and the output matching network need to be reconfigured with the signal envelope.

From the above discussion it emerges that an important feature of the TMN is the speed necessary to set a certain impedance state. From this point of view there are two possibilities: i) slow impedance setting rate: this implies narrow-band modulation signals and static reconfiguration of the output power; ii) fast impedance setting rate: wide-band modulation signals can be used and the amplifier has the capability to fully track the signal envelope.

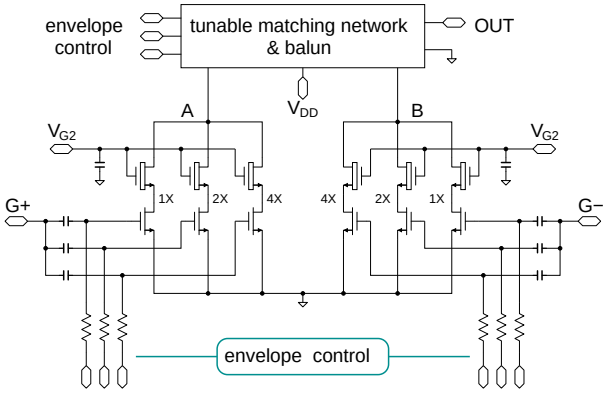


Fig. 2. Simplified schematic of the PA core (final stage only). The envelope control signals are used to adjust both the transistor size and the output matching network. The circuit can be divided in PA core and tunable matching network.

The final stage of the proposed PA is illustrated in Fig. 2 and exploits a push-pull configuration in 65 nm CMOS technology. Each power device is composed by three branches of increasing widths. These branches are connected in AC (i.e. the source and drain terminals are wired together while gate pins are connected through DC-block capacitors) but each one can be switched on and off with a mere control of their (bias) gate potentials. This means that, as a function of the voltage applied to the envelope control inputs, the overall biasing current of the final stage can be dynamically varied. In particular, since the transistor widths follow the 1, 2, 4 geometrical series (i.e. $W_2 = 2W_1$ and $W_4 = 2W_2 = 4W_1$), the bias current can be varied from a certain value, say I_0, when only the small device is switched

on, to $7I_0$ if all the devices are activated. The first condition will be referred as the $1\times$ state (minimum transistor width) whereas the last one is referred as the $7\times$ state (maximum transistor width). All the intermediate states are, of course, possible. As a result the 1 dB compression point of the amplifier can be dynamically varied in order to track the modulation envelope.

Each device branch is composed by a cascode of two transistors as reported in Fig. 3. This choice has been dictated by two reasons. First, the cascode connection improves the breakdown voltage of the pair with respect to that of a single MOS transistor. For this reason the top transistor is a 1.8 V, thick-oxide device. Second, the cascode significantly reduces the intrinsic capacitance seen between the drain and the gate of output (common-gate) and input (common-source) devices respectively. As a result the amplifier stability is improved, whereas the input matching does not depend (too much) on the load impedance. The latter property is particularly useful when dealing with an output TMN, as in the present case.

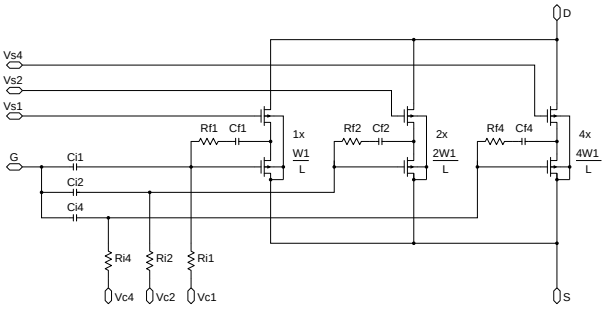


Fig. 3. Reconfigurable MOS transistor (3-cells) with RC feedback networks and gate 1 resistances for stabilization. The input signals are capacitively coupled to the gate 1 of each cascode cell. The common-gate transistors are 1.8 V thick-oxide devices. $W_1 = 480\,\mu$m, $L = 65$ nm.

During the design of the PA core a particular attention has been paid to the parasitic output capacitance of the transistors. Indeed, when one of the three branches is switched-off, its drain-to-source capacitance remains in parallel to the device output. Such an effect must be accurately modeled in order to estimate both the stability performances and the small-signal gain of the reconfigurable transistor in the different states. Secondly also the input impedance varies when a cell is switched on and off. However such an effect is negligible, thank to the cascode connection.

Another aspect that has been studied in depth is the amplifier stability. To this purpose an internal stabilization circuitry is essential. In order to stabilize the device two well-known techniques have been adopted, namely: i) RC feedback, see R_f and C_f in the schematic of Fig. 3, and ii) resistive loading of the gate terminals, see R_i in the same schematic. It is worth noticing here that the RC feedback is applied only to the common-source stage of each branch. In this way, when a certain branch is set in the off state, the relative RC feedback circuit isolated from the other portions of the discrete-resizing device. This effect is achieved because, to switch-off a certain branch, also the common-gate (i.e. top) transistor is switched-off. As a result the stabilization circuit of a switched-off branch does not load the device elements that are still active.

The adopted design methodology starts from the device sizing needed for the required output power. This first step has been carried-out assuming a deep AB-class biasing with $V_{dd} = 2.2$ V, $V_{g1s} = 0.6$ V and $V_{g2} = 2$ V (note that the breakdown voltage is 2.5 V for the thin-oxide devices and 3.5 V for the thick-oxide devices). The output power ranges from 21 dBm in the $1\times$ state to about 29 dBm in the $7\times$ state. The first-guess sizing has been done by exploiting the load-line theory as in [25] and simple scaling rules.

Once the discrete-resizing devices have been sized and stabilized, they have been characterized by extensive load-pull simulations. This has been done using the HB solver of the ADS software, in conjunction with the CMOS foundry design-kit. Such an analysis allowed us to determine the load impedances corresponding to the maximum PAE points of the discrete-resizing amplifier, i.e., the optimum load impedances. These impedances are referred to the (differential) terminals AB shown in Fig. 2 and are derived under the assumption that an ideal 1:1 balun transformer is used to bias the drain terminals of the push-pull stage.

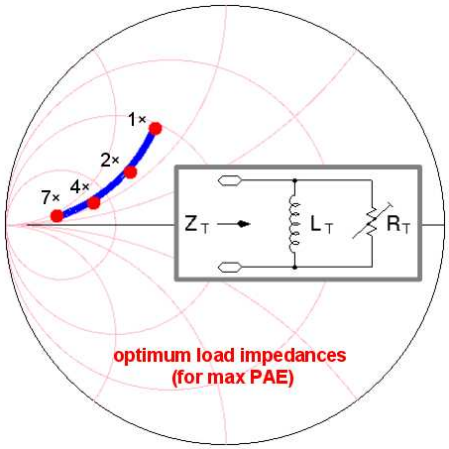


Fig. 4. Optimum load impedances for maximum PAE (a) and load equivalent circuit (b). For each state of the reconfigurable transistors a different optimum load is needed (red circles). The low impedance point corresponds to the $7\times$ state whereas the high impedance point is obtained in the $1\times$ state. These loads can be described by means of a variable resistor R_T (in the range $6.8 - 46\,\Omega$) in parallel to a fixed inductor $L_T = 2.3$ nH (blu line). At 2.45 GHz the inductor resonates-out the output 1.8 pF capacitance of the transistors.

The optimum load impedances for the operating frequency of 2.45 GHz are reported in Fig. 4. It can be noticed that, as the transistors are progressively switched-on and the state changes, these impedances follow quite precisely a constant susceptance coordinate contour, thus indicating that a very simple load model can be assumed (see

inset of Fig. 4). Such a model uses a variable resistor R_T (in the range from 6.8 to 46 Ω) in parallel to a fixed inductor $L_T = 2.3$ nH (blue line). The resistor describes the power delivered to the load and its value is a function of the effective transistor width W_t. In particular R_T is inversely proportional to W_t, i.e. it decreases as W_t increases from the 1× to the 7× state. The inductor L_T, instead, is required to resonate-out the output capacitance C_{out} of the discrete-resizing devices at the center frequency of the PA. Here is interesting to note that C_{out} is almost constant and independent of the switching state, this because C_{out} is dominated by the drain-to-bulk parasitic capacitances of the common-gate transistors. Fitting the above load model to the optimum load impedances a value $L_T = 2.3$ nH is obtained. This indicates that $C_{out} \approx 1.8$ pF.

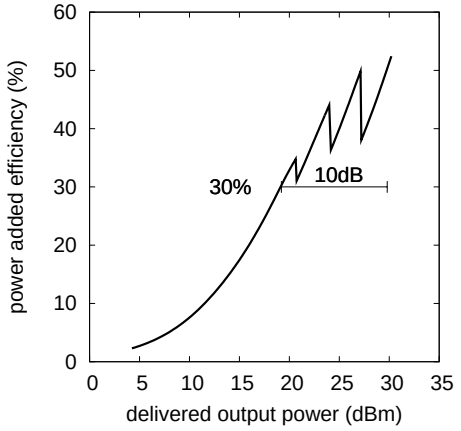


Fig. 5. Simulation of the whole PA-core. The PAE is plotted versus output power, ideally combining all the switching states together. A PAE better than 30 % can theoretically be obtained at about 10 dB back-off from the maximum power. This requires a low-loss tunable matching network.

The design of the PA core (the details of which are outside the scope of the present paper) has then been completed adding an input matching network designed for maximum power transfer and a class-AB driver amplifier. The PAE of the whole amplifier (i.e. driver + final stages) is shown in Fig. 5. Such a graph has been obtained combining all the resizing-states, i.e. assuming a discrete control as a function of the output power (signal envelope). This means that, when the output power is above a certain threshold, the transistor size is increased in order not to worse the amplifier linearity while keeping an overall good efficiency. As it can be seen from the figure, a PAE better than 30 % can be theoretically obtained, even at 10 dB back-off from the maximum power. The other amplifier performances are summarized in Tab. 1.

state	W_t (mm)	gain (dB)	PAE (%)	$P_{1\text{dB}}$ (dBm)
1×	0.48	19.2	35	21.0
2×	0.76	21.7	45	24.1
4×	1.28	23.3	50	27.1
7×	2.52	25.5	51	29.4

Tab. 1. Simulated performances of the PA core versus the resizing state. W_t is referred to the thin-oxide devices.

From the previous discussion it is possible to conclude that ET and discrete-resizing PA can be combined to solve the efficiency-linearity bottleneck, i.e. to improve the average power efficiency also in the presence of modulation formats with high envelope Peak-to-Average Ratio. To let the proposed approach viable, however, a TMN should be used in conjunction with the reconfigurable amplifier. The design of such a network will be treated in the next section.

3. TMN Design

The proposed TMN aims at minimizing the insertion losses as much as possible, thus an off-chip solution based on high Q-factor RF-MEMS capacitors has been chosen [26]. Another advantage of the RF-MEMS technology is the very low third-order intermodulation. Passive third-order Input Intercept Points (IIP_3) greater than +60 dBm have been reported for these devices, together with a power handling capability around +36 dBm for miniature packages. The disadvantage of the RF-MEMS technology is the relatively high settling time (in the order of 50 μs), thus in the present work we will only focus on narrow-band modulation signals and static reconfiguration of the PA.

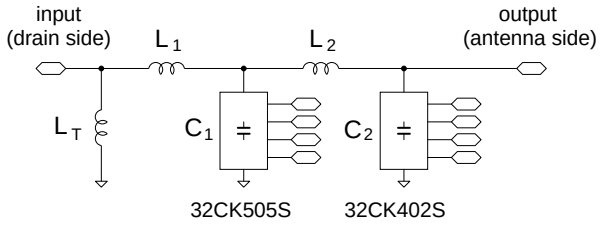


Fig. 6. Simplified schematic of the tunable matching network, implemented with a two-stages ladder structure. In the schematic L_T is the inductance required to resonate-out, at the operating frequency, the output capacitance of the discrete-resizing transistors.

The schematic of the designed network is shown in Fig. 6. According to [24] it is based on a two-stage ladder network (i.e. two L stages in cascade). Such an architecture has been selected since it is characterized by a low complexity, a good compactness and relatively low insertion losses (at high impedance transfer ratio, i.e. in the worst condition) even with moderate capacitor Q-factors. The main principle behind the two stage ladder network, indeed, is that the impedance transformation is obtained in two jumps, thus minimizing the losses for a given component quality. In particular if Z_l is the load impedance (transmitter antenna side, 50 Ω in our case), and Z_i is the input impedance that must be synthesized (transistor drain side), the intermediate impedance Z_p can be designed in order to ensure the same impedance ratio between the two stages:

$$\frac{Z_l}{Z_p} = \frac{Z_p}{Z_i} \tag{1}$$

This design principle is adopted as the main guideline in order to optimize the TMN performances at the high transfer

ratio. The TMN circuit elements are two inductors (L_1 and L_2) and two variable capacitors (C_1 and C_2). The inductance L_T, instead, is required to resonate-out, at the operating frequency, the output capacitance of the discrete-resizing transistors.

The selected devices are commercial products from the Cavendish Kinetics biased at 1.8 V and digitally controlled through a simple 3-wire (SPI compatible) interface. There are two capacitor models available: the 32CK505S type [22] with the capacitance ranging in the interval $1.1-5.1$ pF and the 32CK402S type [23] with the capacitance ranging in the interval $0.6-2.0$ pF. Both intervals can be covered in 32 steps (i.e. 5-bit control words) with 129 fF and 45 fF step size for the 32CK505S and 32CK402S devices respectively. Both Digital Variable Capacitors (DVCs) are bumped bare CMOS dies with integrated charge pump and control logic, of about 2 mm^2 size and a height of 400 μm. These dies can be directly mounted on a printed circuit board. The Q-factor at 2.45 GHz is greater than 40 for the 32CK505S type programmed at the maximum capacitance and greater than 80 for the 32CK402S type. The measurements of the low-frequency capacitances versus the state are reported in Fig. 7 showing that, in both cases, it is possible to increase the capacitance in a very linear fashion. The measurements have been done at 10 MHz with the HP-4275A RLC meter.

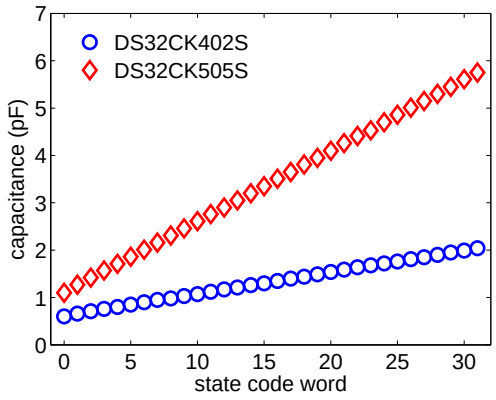


Fig. 7. Low-frequency capacitance measured as a function of the RF-MEMS state (i.e. of the digital code word used to control the capacitor).

In order to design the TMN, the capacitor parasitics must be determined. Fig. 8(a) shows the capacitor equivalent circuit. In this model C is the low-frequency capacitance. In the case of the adopted RF-MEMS devices this capacitance can be varied as described above. The other two device parasitics are the inductance L_s and the resistance R_s. L_s accounts for both the package and the via-ground inductances and is responsible for the self-resonance frequency of the device. R_s models the capacitor losses and, thus, determines the Q-factor of the capacitor. Fig. 8(b) shows the capacitance versus the frequency (i.e. the frequency response of the device) including the parasitic. The curve with the circular symbols has been obtained exploiting the factory design-kit of the 32CK505S capacitor and considering the state 18, corresponding to $C = 3.44$ pF. As it can be seen, because of the parasitic inductance, the equivalent capacitance of the device increases with frequency. For the same reason, the Q-factor (not shown in the figure) decreases with frequency.

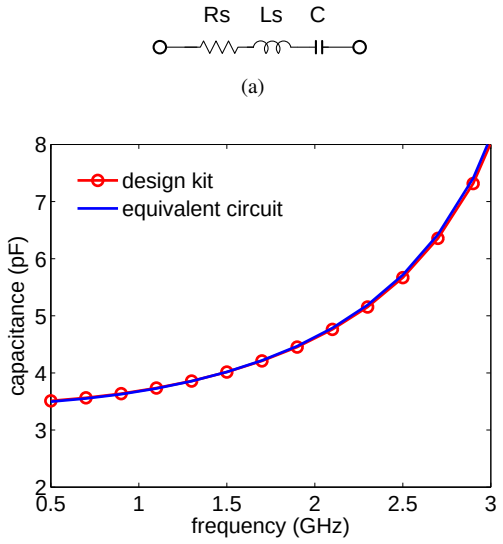


Fig. 8. Equivalent circuit of the digitally-controlled RF-MEMS capacitors (a) and corresponding frequency response (b). The 32CK505S device from Cavendish Kinetics is considered in the graph. The frequency response is obtained plotting the equivalent capacitance versus the frequency and comparing the design kit model (provided by the device manufacturer) with the equivalent circuit in (a). The equivalent circuit parameters are: $C = 3.44$ pF; $L_s = 0.5$ nH and $R_s = 0.4\,\Omega$. The parasitic inductance includes the via hole ground connections and the tracks on the board: these effects contribute for about 0.4 nH. The low frequency capacitance C corresponds to the code word 18.

The parameters of the equivalent circuit have been determined by means of a fitting procedure (on both C and Q versus the frequency). The results are reported in Fig. 8(b) with a solid line. Using this procedure the following estimation is obtained: $L_s = 0.5$ nH and $R_s = 0.4\,\Omega$. The same study has been repeated for the 32CK402S with similar results.

The next design step is the sizing of the TMN elements. This has been done according to (1) for the largest tuning ratio and using a CAD optimization to cover the region of the Smith's chart where the optimum load impedances are located (see Fig. 4). At the end of the design procedure the tuning-law reported in Tab. 2 is obtained.

state	C_1 (pF)	C_2 (pF)	L_T (nH)	L_1 (nH)	L_2 (nH)
1×	1.00	0.60	2.3	1.0	2.6
2×	1.75	0.95	2.3	1.0	2.6
4×	2.65	1.25	2.3	1.0	2.6
7×	2.80	0.65	2.3	1.0	2.6

Tab. 2. Tuning law of the reconfigurable matching network at 2.45 GHz, (simulations).

In the first step the TMN has been designed exploiting lumped components. In order to reduce the inductor losses, however, these have been implemented as distributed components in microstrip technology. To this purpose the well-known semi-lumped method is adopted. This method relies on the following approximation:

$$L \approx Z_c \tan\left(\frac{2\pi l}{\lambda}\right) \tag{2}$$

where Z_c, λ and l are the characteristic impedance the wavelength and the physical length respectively of the microstrip line used to implement the inductances. The above approximation works well if $l \ll \lambda$ (in practice $l \leq \lambda/10$). If this approach is adopted the length values quoted in Tab. 3 are obtained and the TMN layout can be drawn.

parameter	inductance (nH)	length (mm)	width (mm)
L_T	2.3	3.3	0.2
L_1	1.0	1.8	0.3
L_2	2.6	4.4	0.2

Tab. 3. Physical dimensions of the semi-lumped inductors implemented in microstrip technology. The substrate height is $h = 0.81$ mm, with a relative permittivity $\varepsilon_r = 3.56$ and a loss tangent $\tan\delta = 0.004$ (material Rogers 4003). The metal is copper ($\sigma = 5.8 \times 10^7$ S/m) with a thickness $t = 35\,\mu$m. The obtained values are referred to the center frequency of 2.45 GHz.

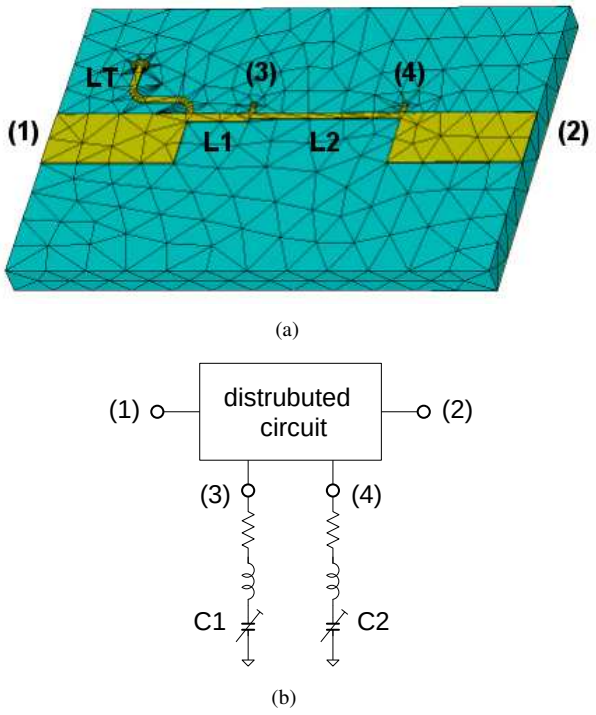


Fig. 9. TMN layout imported by the electromagnetic simulator (a) and CAD model (b). The PCB has a length of 14 mm and a width of 9.4 mm. The RF-MEMS capacitors are connected to ports (3) and (4). The output (antenna side) is at port (2). The input (transistor drain side) is at port (1).

As a final design step, the TMN layout is synthesized and analyzed with the CST electromagnetic simulator. Fig. 9(a) shows a 3D view of such a layout implemented within the CST software. The full-wave simulation is performed by using the frequency domain solver with a tetrahedral mesh. Fig. 9(a) refers only to the starting mesh generated before the simulation; the final mesh consists of about 30000 cells.

At this point it is important to note that the distributed TMN structure has been defined as a four-ports circuit. The output (antenna side) is at port (2). The input (transistor drain side) is at port (1). The RF-MEMS capacitors C_1 and C_2 are connected to ports (3) and (4) respectively. After the electromagnetic analysis, the 4-ports scattering parameters file (Touchstone format) is imported within the ADS CAD software and the capacitor equivalent circuits are connected to the corresponding ports, see Fig. 9(b). This allows for a very accurate co-simulation of the TMN and for the fine tuning of the design.

The overall TMN performances at the end of the design phase are quoted in Tab. 4. This table shows that the TMN input impedances Z_i are in close agreement with the optimum load impedances Z_t required by the discrete-resizing PA.

state	Z_T (Ω)	Z_i (Ω)	G_p (dB)
1×	$18.2 + j22.7$	$18.0 + j21.9$	-0.26
2×	$18.0 + j11.4$	$18.1 + j11.5$	-0.40
4×	$12.3 + j3.9$	$12.3 + j3.8$	-0.74
7×	$6.5 + j1.3$	$6.5 + j1.3$	-0.88

Tab. 4. Simulated performances of the reconfigurable matching network at 2.45 GHz. Z_T is the target impedance, i.e. that required by the PA at each state; Z_i is the input impedance, i.e. that synthesized by the network; G_p is the operating power gain achieved.

The estimation of the TMN power gain is also shown in Tab. 4. Following [24] and other authors, the operating power gain G_p has been used as the figure of merit to describe the insertion losses of the circuit. G_p can be expressed with the following relationship:

$$G_p = \frac{|S_{21}|^2}{1 - |S_{11}|^2} \tag{3}$$

where S_{ij} with $i, j = 1, 2$ are the scattering parameters of the TMN measured with respect to a common reference impedance (e.g. $Z_0 = 50\,\Omega$) at both input and output ports.

4. Results

Once the design has been completed the Gerber files of the circuits have been set to a PCB manufacturer and the prototypes have been fabricated exploiting a Rogers 4003 substrate ($\varepsilon_r = 3.56$ and $h = 0.81$ mm). The RF-MEMS capacitors, with miniature, flip-chip type package have been

provided by Cavendish Kinetics and mounted on the PCBs by Tesla. The assembled circuits are shown in Fig. 10. In the left panel of this figure it is possible to see the completed TMN, whereas the right panel represents the test jig of a single RF-MEMS capacitor, mostly used to verify the control firmware (see Fig. 7). Such a firmware has been implemented exploiting an "Arduino UNO" micro-controller [27] and can be used to program both the capacitors of the TMN.

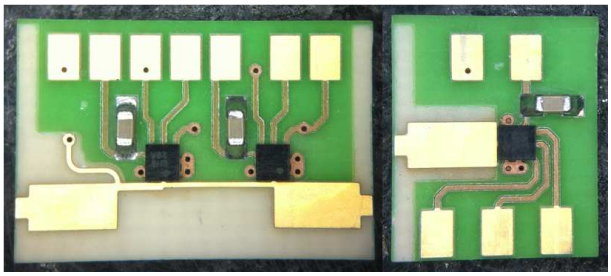
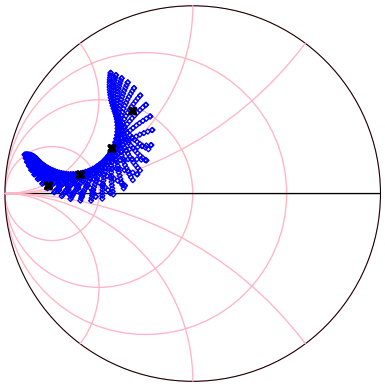
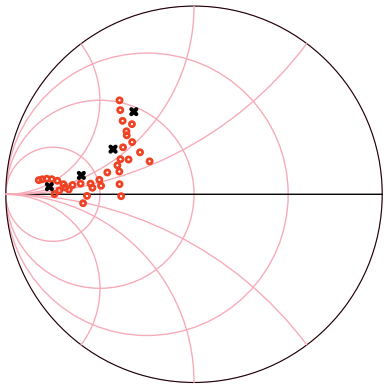


Fig. 10. Implemented prototypes: tunable matching network (left) RF-MEMS capacitor test jig (right). The PCBs have been fabricated exploiting the Rogers 4003 substrate.



(a) simulations

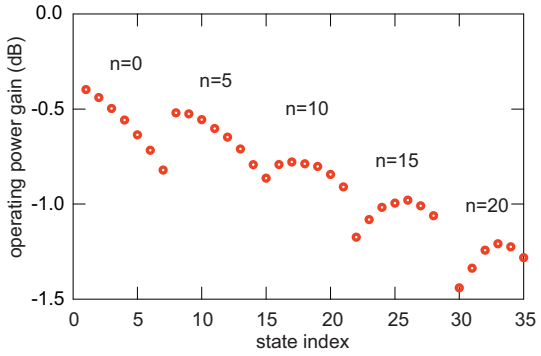


(b) measurements

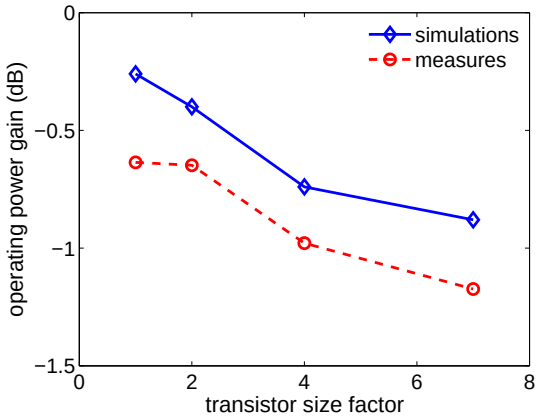
Fig. 11. Simulated (a) and measured (b) Smith's chart coverage provided by the TMN. During the measurements C_1 and C_2 have been varied with steps 5 times greater than the minimum capacitive increment. These values correspond to about 645 fF for C_1 and to 225 fF for C_2.

The electrical performances of the TMN have been measured using a Wiltron test fixture (3680 K model) and a 40 GHz Agilent vector network analyzer (PNA N52230A model). By a careful calibration, the reference planes of the structure have been referred to the end of the 50 Ω launching microstrips connected to both port (1) and (2). The calibration standard is constituted by two microstrip opens having a 3.9 mm physical length, i.e. the same length of the launching microstrip sections. The calibration standard is implemented with the same substrate used for the TMN. The same reference planes have been assumed in the simulations.

The simulated and measured impedances seen at port (1) are illustrated in Fig. 11(a) and in Fig. 11(b) respectively. Each point represents a different setting of the code words used to program C_1 and C_2. As it can be seen, there is a good agreement between simulation and measurements. Moreover the implemented TMN is capable to reach all the target impedances (cross symbols in the above figures).



(a) G_p vs capacitors state



(b) G_p vs transistor state

Fig. 12. Operating power gain G_p versus capacitors (a) and discrete-resizing transistor state (b). The target impedances can always be reached with a G_p better than 1.5 dB.

In order to obtain the graph of Fig. 11(b), C_1 and C_2 have been varied with steps 5 times greater than the minimum capacitive increment. In particular, for a given C_1, C_2 is varied between its minimum and maximum capacitance; then C_1 is increased and the cycle is repeated. To simply model this setting procedure, the state code words of C_1 and C_2 can be represented by the integer numbers n and m respectively. Now, since the measurements have been carried-out at steps of five, these numbers can assume

only a limited set of values i.e. $n = 0, 5, 10, 15, 20$ and $m = 0, 5, 10, 15, 20, 25, 30$. Note that m is limited to 30 since, with 5-bits, the code words are in the range 0-31. On the other hand n is limited to 20 since the corresponding C_1 is sufficient to reach the lower target impedances.

The operating power gain of the TMN has been derived from the measured scattering parameters exploiting (3). The obtained results are plotted in Fig. 12(a) as a function of the state index i. Such an index has been defined combining the code words n and m of the two capacitors:

$$i = 7\left(\frac{n}{5}\right) + \left(\frac{m}{5}\right) + 1. \tag{4}$$

From the analysis of this graph it emerges that all the target impedances can be reached with a G_p greater than -1.5 dB (i.e. insertion losses lower than 1.5 dB). Finally Fig. 12(b) compares the operating power gain simulations with the measurements. The values are reported as a function of the discrete-resizing transistor state W_t/W_1, i.e. the effective transistor width normalized to that of the $1\times$ state. The agreement between simulations and measurements is within 0.5 dB. A discrepancy of about 0.2 dB can be attributed to the fixture insertion losses that are not calibrated-out measuring a simple open standard.

5. Conclusions

In this work, for the first time, a tunable matching network based on digitally-controlled RF-MEMS capacitors and suitable for envelope-tracking discrete-resizing power amplifiers has been proposed, designed and experimentally validated. The circuit exploits a two-stages ladder architecture and has been implemented on a tiny PCB having a length of 14 mm and a width of 9.4 mm. The tunable matching network operates at 2.45 GHz and the RF-MEMS capacitors are commercial devices from Cavendish Kinetics. They are biased at 1.8 V and digitally controlled through a simple 3-wire (SPI compatible) interface. The firmware has been implemented in a low-cost "Arduino UNO" microcontroller and it can be used to program the capacitors. The fabricated prototype allows a 50 Ω load to be transformed into a lower impedance, the magnitude of which is in the range $8.4 - 28\,\Omega$. In such a range the insertion loss is always better than 1.5 dB and thus the proposed TMN is suitable for watt-level discrete-resizing CMOS PAs.

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